# ***Name : RAHUL GOEL***

# ***Reg No : RA1911030010094***

# ***Section: O2***

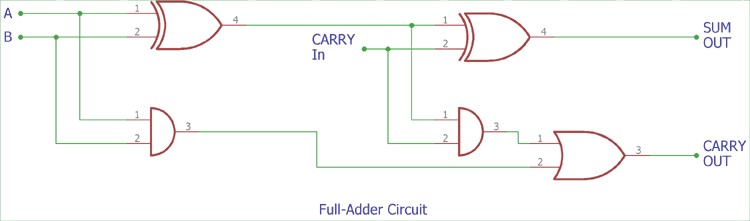
# Ex.8.FULL ADDER CIRCUIT

**AIM** : To design and implement a full adder **circuit.SOFTWARE USED** : Logic gate simulator

**TRUTH TABLE** :

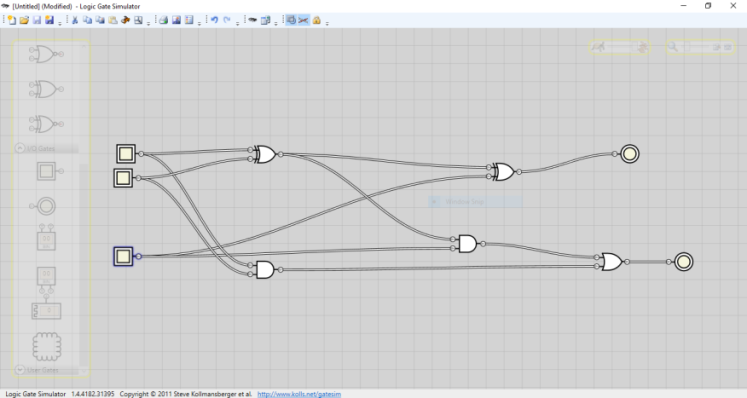
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| INPUTS | | | OUTPUTS | |
| A | B | C-IN | C-OUT | S |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**CIRCUIT DIAGRAM** :

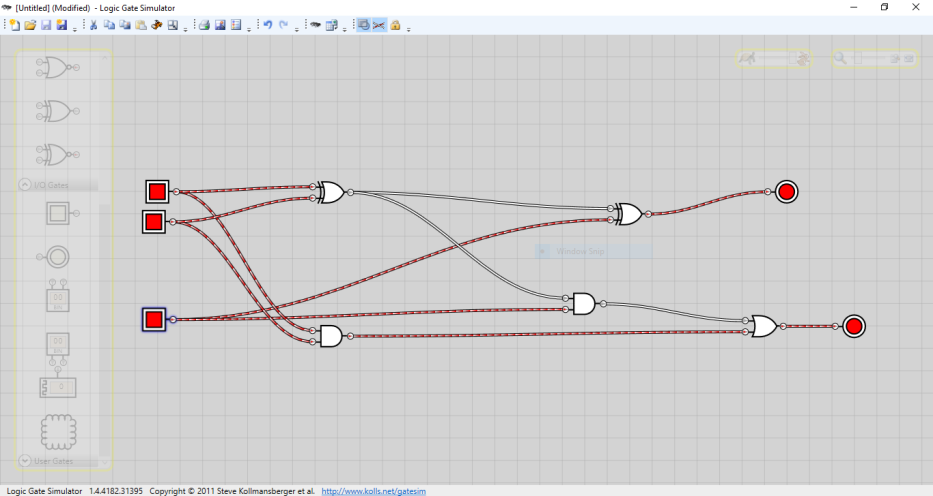


**OUTPUT** :

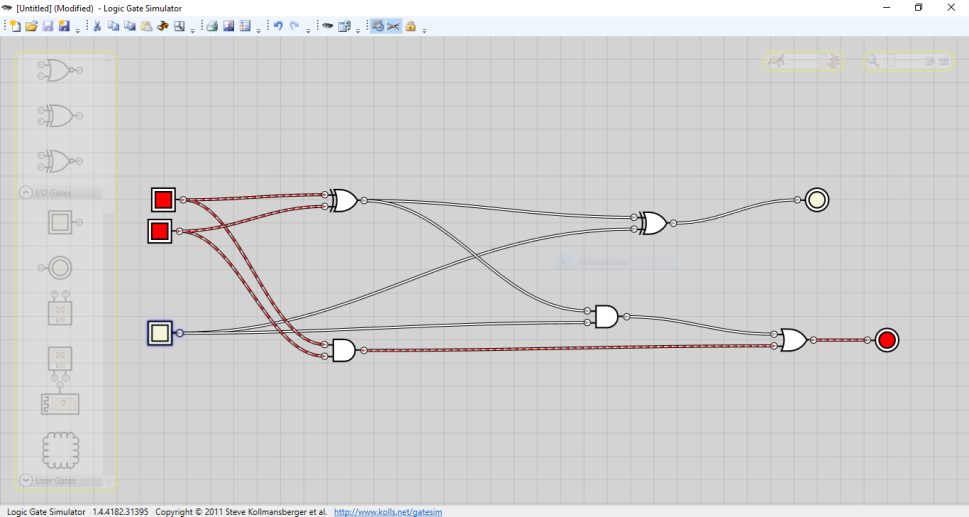
1)



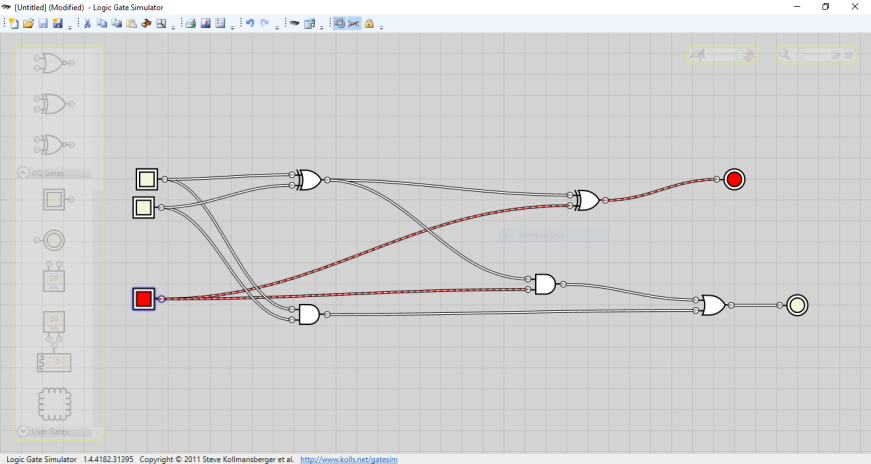
2)



3)



4)



**RESULT** :

***Here, we add three one bit binary numbers, two operands & a carry bit.***